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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,913	11/13/2003	Soon Sung Yoo	8733.935.00-US	7322

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EXAMINER	
TOBERGTE, NICHOLAS J	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 02/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

HA

Office Action Summary	Application No.	Applicant(s)	
	10/705,913	YOO ET AL.	
	Examiner	Art Unit	
	Nicholas J. Tobergte	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-7 and 10-14* is/are pending in the application.

4a) Of the above claim(s) *1,2,8,9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-7 and 10-14* is/are rejected.

7)☒ Claim(s) [redacted] is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/22/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group II claims 3-7 and 10-14 in the reply filed on 12/2/2005 is acknowledged.

Claim Rejections - 35 USC § 112

Claim 3 recites the limitation "on the low part" in claim 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Objections

Claims 6 and 13 are objected to because of the following informalities: The applicant claims in claims 6 and 13 the following: "forming the gate insulation pattern and the protection film pattern ***using*** the protection film pattern and the insulation film using the photoresist pattern." The examiner requests that the applicant clarify this claim, as the examiner believes that this is not physically possible. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 3,6,7,10,13 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Ueda et al (US 6,078,365).

Pertaining to claim 3, Ueda teaches a method of manufacturing a thin film transistor array substrate, comprising:

forming using a first mask process, a gate electrode **G** of the thin film transistor on the substrate **71**, a gate line **63** connected to the gate electrode **G**, a gate pattern including the gate pad **68** connected to the gate line **Col 21 line 8 to Col 22 line 13**;

forming a gate insulation film **76** on the substrate where the gate pattern is formed **Col 22 lines 14-18**;

forming using a second mask **Col 22 line 22** process a source electrode **S** and a drain electrode **X** of the thin film transistor on the gate insulation film, a data line **62** connected to the source electrode **S**, a data pad **Col 24 lines 11-19** connected to the data line **62**, a source/drain pattern including a storage electrode **Col 19 lines 48-61** in the region superimposed with the gate line **63**, and a semiconductor pattern formed corresponding to the source/drain pattern on the low part; and

forming using a third mask process a pixel electrode **61** connected to the drain electrode **X** and the storage electrode , a gate pad protection electrode **79** formed to cover the gate pad, a transparent electrode pattern **81** including the data pad protection electrode formed to cover the data pad **Col 24 lines 11-30**, and a gate insulation pattern **76** and a protection film pattern **77** stacked in the a region other than the region where the transparent electrode pattern is formed **See Figure 25c and Diagram below**.

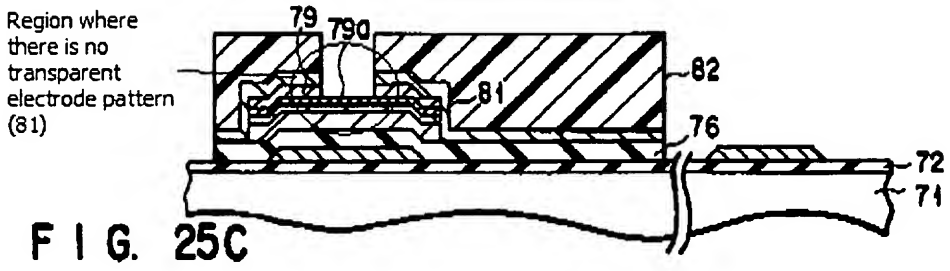

Figure 25c Diagram

Pertaining to claim 6, Ueda teaches the method of manufacturing the thin film transistor array substrate according to claim 3, wherein the third mask process comprises:

forming a protection film **81** on the substrate where source/drain pattern is formed **Col 22 lines 23-28**;

forming the photoresist pattern using the third mask **Col 22 line 32**;

forming the gate insulation pattern **76** and the protection film pattern **81** using the protection film pattern and the insulation film using the photoresist pattern;

evaporating **Col 22 line 30** a transparent electrode material **81** on the substrate where the photoresist pattern exists **Col 22 line 32**; and

forming the transparent electrode pattern **81** by removing the photoresist pattern by strip process and the transparent electrode material **Col 22 lines 35-38**.

Pertaining to claim 7, Ueda teaches the method of manufacturing the thin film transistor array substrate according to claim 3, wherein the protection film pattern **81** partially

exposes the drain electrode **X, 79** and the storage electrode **Col 19 lines 48-61** and is connected to the pixel electrode **61**. **See Figure 23C.**

Pertaining to claim 10, Ueda teaches a method of manufacturing a thin film transistor array substrate, comprising:

forming using a first mask process, a gate electrode **G** of the thin film transistor on the substrate **71**, a gate line **63** connected to the gate electrode **G**, a gate pattern including the gate pad **68** connected to the gate line **Col 21 line 8 to Col 22 line 13**;

forming a gate insulation film **76** on the substrate where the gate pattern is formed **Col 22 lines 14-18**;

forming using a second mask **Col 22 line 22** process a source electrode **S** and a drain electrode **X** of the thin film transistor on the gate insulation film, a data line **62** connected to the source electrode **S**, a data pad **Col 24 lines 11-19** connected to the data line **62**, a storage electrode superimposed over the gate line **63**; and

forming a pixel electrode **61** using a third mask process connected to the drain electrode **X** and the storage electrode **Col 19 lines 48-61**, a gate pad protection electrode **79** formed to cover the gate pad, a transparent electrode **81,** a data pad protection electrode covering the data pad **Col 24 lines 11-30**, and a gate insulation pattern **76** and a protection film pattern **77** stacked in the a region other than the region where the transparent electrode is formed **See Figure 25c and Diagram above**.

Pertaining to claim 13, Ueda teaches the method of manufacturing the thin film transistor array substrate according to claim 3, wherein the third mask process comprises:

forming a protection film **81** on the substrate where the storage electrode **Col 19 lines 48-61** is formed **Col 22 lines 23-28**;

forming the photoresist pattern using the third mask **Col 22 line 32**;

forming the gate insulation pattern **76** and the protection film pattern **81** using the protection film pattern and the insulation film using the photoresist pattern;

evaporating **Col 22 line 30** a transparent electrode material **81** on the substrate where the photoresist pattern exists **Col 22 line 32**; and

forming the transparent electrode pattern **81** by removing the photoresist pattern by strip process and the transparent electrode material **Col 22 lines 35-38**.

Pertaining to claim 14, Ueda teaches the method of manufacturing the thin film transistor array substrate according to claim 10, wherein the protection film pattern **81** partially exposes the drain electrode **X, 79** and the storage electrode **Col 19 lines 48-61** and is connected to the pixel electrode **61**. **See Figure 23C.**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda et al as applied to claim 3 above, and further in view of Choi et al (US 6,958,788).

Pertaining to claim 4, Ueda teaches the method of manufacturing the thin film transistor array substrate according to claim 3, but fails to teach wherein the second mask process uses a diffraction exposure mask having the diffraction exposure part in the channel part of the thin film transistor.

Choi shows that using a diffraction mask when exposing the channel region is well known to provide small device features such as channels on a TFT **Col 2 lines 40-44.** Therefore it is obvious to one of ordinary skill in the art to apply the teaching of Choi to that of Ueda when forming the channel regions of a TFT.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda et al as applied to claim 3 above, and further in view of Choi et al and Parks et al (US 4,855,806).

Pertaining to claim 5, Ueda teaches the method of manufacturing the thin film transistor array substrate according to claim 3, including:

sequentially forming a semiconductor layer **77**, and a source/drain metal layer **79** on the gate insulation film **76**;

but fails to teach wherein the second mask process comprises:

forming by use of the diffraction exposure mask a photoresist pattern where the channel part of the thin film transistor has a height lower than the source/drain pattern part;

patterning the source/drain metal layer and the semiconductor layer by use of the photoresist pattern;

ashing the photoresist pattern to a prescribed depth;

removing a source/drain metal layer of the channel part of the thin film transistor by use of the ashed photoresist pattern; and

removing the photoresist pattern by a strip process.

Choi teaches:

forming by use of the diffraction exposure mask a photoresist pattern where the channel part of the thin film transistor has a height lower than the source/drain pattern part;

patterning the source/drain metal layer and the semiconductor layer by use of the photoresist pattern; **Col 2 lines 38-47**

Parks teaches:

ashing the photoresist pattern to a prescribed depth;

removing a source/drain metal layer of the channel part of the thin film transistor by use of the ashed photoresist pattern; and

removing the photoresist pattern by a strip process. **Col 6 lines 50-56**

Therefore it would have been obvious to one of ordinary skill in the art to combine the references of Parks and Choi into the teachings of Ueda. The motivation for this is twofold. Parks shows that ashing of a photoresist in a transistor fabrication process, particularly when forming a metal layer, has been well known in the art for a long time, and that it toughens the metal layer prior to etching. Choi shows that the use of a diffraction mask when forming the channel region, including the limitation of having a photoresist pattern part (which is what forms the channel) with a height lower than the height of the source/drain pattern and storage pattern is well known and directly applys to the formation of a TFT as taught by Ueda. The motivation is that a diffraction mask is well known in the art for forming channels.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda et al as applied to claim 3 above, and further in view of Choi et al (US 6,958,788).

Pertaining to claim 11, Ueda teaches the method of manufacturing the thin film transistor array substrate according to claim 10, but fails to teach wherein the second mask process uses a diffraction exposure mask having the diffraction exposure part in the channel part of the thin film transistor.

Choi shows that the use of a diffraction mask when forming the channel region, including the limitation of having a photoresist pattern part (which is what forms the channel) with a height lower than the height of the source/drain pattern and storage pattern is well known and directly applys to the formation of a TFT as taught by Ueda

Col 2 lines 40-44. Therefore it is obvious to one of ordinary skill in the art to apply the teaching of Choi to that of Ueda when forming the channel regions of a TFT.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda et al as applied to claim 10 above, and further in view of Choi et al and Parks et al (US 4,855,806).

Pertaining to claim 12, Ueda teaches the method of manufacturing the thin film transistor array substrate according to claim 10, wherein the second mask process comprises:

sequentially forming a semiconductor layer **77 78**, and a source/drain metal layer **79** on the gate insulation film **76**;

But fails to teach:

forming by use of the diffraction exposure mask a photoresist pattern where the channel part of the thin film transistor has a height lower than the storage electrode;

patterning the source/drain metal layer and the semiconductor layer using the photoresist;

ashing the photoresist to a prescribed depth;

removing a source/drain metal layer of the channel part of the thin film transistor by use of the ashed photoresist; and

removing the photoresist by a strip process.

Choi teaches:

forming by use of the diffraction exposure mask a photoresist pattern where the channel part of the thin film transistor has a height lower than the source/drain pattern part;

patterning the source/drain metal layer and the semiconductor layer by use of the photoresist pattern; **Col 2 lines 38-47**

Parks teaches:

ashing the photoresist pattern to a prescribed depth;

removing a source/drain metal layer of the channel part of the thin film transistor by use of the ashed photoresist pattern; and

removing the photoresist pattern by a strip process. **Col 6 lines 50-56**

Therefore it would have been obvious to one of ordinary skill in the art to combine the references of Parks and Choi into the teachings of Ueda. The motivation for this is twofold. Parks shows that ashing of a photoresist in a transistor fabrication process, particularly when forming a metal layer, has been well known in the art for a long time, and that it toughens the metal layer prior to etching. Choi shows that the use of a diffraction mask when forming the channel region, including the limitation of having a photoresist pattern part (which is what forms the channel) with a height lower than the height of the source/drain pattern and storage pattern is well known and directly applys to the formation of a TFT as taught by Ueda. The motivation is that a diffraction mask is well known in the art for forming channels.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nicholas J. Tobergte whose telephone number is 571-272-6006. The examiner can normally be reached on Mon - Thur 7am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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